REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 12 September 2005. Responsive to the rejections to the Claims made in the Official Action, Claims 1, 7, and 13 have been amended to further clarify the combination of elements defining the present invention.

In the Official Action, the Abstract of the Disclosure was objected to because it exceeded 150 words limit. Accordingly, the Abstract of the Disclosure has been amended to reduce the size of the Abstract to below 150 words, and to improve the language thereof.

Further, in the Official Action, Claims 1-5, 7-11, and 13-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent #6,725,286 granted to Takahachi in view of U.S. Patent #6,131,135 granted to Abramson, et al.

The Takahachi Patent is directed to an information processing apparatus, a memory card, and a program storage medium. A memory card 6 has VSS connected to the ground, a BS pin for receiving a bus-state signal, VCC pins for receiving a voltage over power supply, an interrupt pin for outputting interrupt data, a clock pin for receiving a clock signal, and reserved pins conforming to USB standards. When the memory card is inserted into a personal computer, the reserved pins are connected to a USB host controller IC employed in the personal computer so that serial data conforming to the

USB standards can be exchanged between the memory card and the personal computer. With this configuration, a desired function is added to the memory card.

A memory card 6 which may be an SD card has the components of the configuration shown in Fig. 12, which are identical with those shown in Fig. 5. The memory card either shown in Fig. 5 or in Fig. 12, includes an ASIC (Application Specific Integrated Circuit) 121 or a base-band IC 171, a memory controller IC 127 or a USB interface unit 128. A RAM 122 is used for storing the programs to be executed by the ASIC 121, while a ROM 123 is used for storing one of the programs which is being executed by the ASIC 121, and parameters changing from time to time in the course of program execution.

A CPU 125 executes a variety of ordinary application programs and an OS. A flash memory 126 is used for storing the programs to be executed by the CPU 125 and basically fixed data used as parameters in processing carried out by the CPU 125. Controlled by the CPU 125, the memory controller IC 127 supplies picture data received from the camera unit through the bus 129 to the personal computer 1, and supplies a data command or the like received from the personal computer 1 to the camera unit by way of the bus 121.

By the same token, controlled by the CPU 125, the USB interface unit 128 supplies picture data received from the camera unit through the bus 129 to the personal computer 1 conforming to the USB standards, and supplies a data command or the like

received from the personal computer 1 conforming to the USB standards to the camera unit by way of the bus 129.

Fig. 8 of Takahachi is a diagram showing a typical software stored in the ROM 123 employed in the memory card 6. Device drivers 1 and 2 are software providing upper layer software with a common procedure for making an access. Each device driver itself is stored in the ROM 123 employed by the memory card 6.

With device drivers stored in the ROM 123 employed in the memory card 6, typically, insertion of the memory card 6 into the personal computer 1 triggers an operation to download the object of a device driver into the personal computer 1. Software in the personal computer 1 detects what device has been inserted into the personal computer 1, and downloads a device driver for the already inserted device from the memory card 6.

It is respectfully submitted that Takahachi reference fails to suggest, disclose, or render obvious the structure which the Applicant regards as the invention and which is clearly emphasized now in Claims 1, 7, and 13.

Specifically, in Takahachi, in contrast to the present invention, it is the software in the personal computer which detects what device has been inserted into the personal computer and downloads a device driver needed for the inserted device. As described in Column 7, Line 45, to and further, it is a CPU 11 employed in the personal computer 1 forms a judgment as to whether or not a specific memory card has been inserted into the

personal computer. As the outcome of the judgment formed at the step S1 indicates that the specific memory card has been inserted into the personal computer, the flow of the downloading process goes to a step S2 at which the CPU 11 initializes the memory card and an inserted device.

Then, at the next step S3, the CPU 11 of the personal computer acquires a device category stored in the ROM 123 of the memory card, and the flow chart goes to a step S4 to form a judgment as to whether or not a device driver identified by the device category acquired at the step S3 is required by an application program to be executed by the personal computer 1 serving as the main unit to drive the inserted device. (Column 8, Lines 1-14) If the outcome of the judgment indicates that the device driver identified by the device category is required by the application program to be executed by the personal computer 1 serving as the main unit, the flow of the downloading process goes on to a step S6. At the step S6, the CPU 11 of the personal computer downloads the device driver identified by the device category acquired at the step S3.

If the outcome of the judgment formed at the step S4 indicates that a device driver identified by the device category is not required by the application program executed by the personal computer 1 serving as the main unit, the flow of the downloading process goes on to a step S5 at which the CPU 11 waits for activation of the application program before this downloading process is ended.

As presented in Column 9, Lines 25 and further, the memory controller IC 127 supplies the audio data supplied by the communication unit through the bus 129 to the personal computer 1, and passes on a command or the like received from the personal computer 1 to the communication unit by way of the bus 129. By the same token, controlled by the CPU 125, the USB interface unit 128 supplies the audio data supplied by the communication unit through the bus 129 to the personal computer conforming to the USB standard, and passes on a command or the like received from the personal computer 1 conforming to the USB standards to the communication unit by way of the bus 129.

It is clear that in Takahachi, it is the personal computer is the main unit for judgment which block, e.g., the memory controller IC 127 or the USB interface unit 128 of the memory card to actuate.

In contrast to Takahachi, in the present invention, it is a function of the controller 24 embedded into the memory chip of the memory card to select an SD (or MS) interface 20 or USB interface 22 to control the coupling of the memory card to a USB connector. In the present invention, it is not a function of the personal computer, or other device having USB connector to which the memory card is to be controllably coupled, to judge whether the memory card (such as for example SD and/or MS) or a USB standard to be executed. Quite to the contrary, in the present invention, the judgment of to what interface to be executed, is a function of the memory card itself, specifically it is judged

by the interface control program 26 of the controller 24 embedded into the memory chip 14.

In the original Specification, Page 5, Line 2 from the bottom to Page 6, Line 17, it is clearly presented that when the CD memory card 10 is not inserted in the adaptor 30, the controller 24 inside the CD memory chip 14 will automatically select executing the SD control interface 20 through the interface control program 26.

While, "when the CD memory card 10 is to be inserted into USB slot for use...the controller 24 inside the CD memory chip 14 will activate the USB control interface through the interface control program 26 in order that the SD memory card 10 can be connected to the USB slot for a smooth operation". This feature of the memory card of the present invention clearly presented in the original Specification is now emphasized in Claims 1, 7, and 13, which now include the following limitation:

...wherein said controller embedded into said memory chip selects a respective one of said SD (or MS or memory card) control interface and USB control interface for actuation, thereby controlling the coupling of said memory card to a USB connector... .

This feature is completely missing in Takahachi, which in fact teaches away from such an arrangement, since in Takahachi, this is the function of the personal computer (outside the memory card) to judge whether the memory controller IC 127 or the USB interface 128 is to be executed and to download a respective driver to process data associated with the connected memory controller or the USB interface.

Abramson, et al., another reference cited by the Examiner, is directed to a method and apparatus for coupling multiple USB host controllers to a high speed bus. The computer system described in Abramson, et al. includes a processor 105 coupled to a host bridge 115 by way of host bus 110. The host bridge 115 couples together system memory 120, a high speed interconnect bus, e.g., a PCI bus 130, and a graphic interface 125. The PCI bus 130 provides a communication path between the processor 105 or system memory 120 and one or more peripheral devices 135. The PCI bus 130 further provides a communication path between the processor 105 or system memory 120 and a Dual Universal Serial Bus (USB) host controller chip 139 which includes a bus interface unit BIU 140, USB arbiter 145, and USB host controllers 150, 155, on a single chip of silicon. The BIU 140 requests access to PCI bus 130 when USB arbiter 145 forwards a bus access request from a selected USB host controller 150, 155.

An external arbiter, such as a PCI arbiter in host bridge 115, independently determines when BIU 140 may access PCI bus 130 and when other peripherals 135 are granted access to PCI bus 130. When an external arbiter such as the PCI arbiter in host bridge 115 grants BIU 140 access to PCI bus 130, USB arbiter 145 grants one access request from USB host controllers 150, 155 to forward the PCI bus 140.

It is respectfully submitted that the Abramson, et al. Patent, in contrast to the present invention, is not concerned with memory card integrating the functions of the USB interface, and is believed to be merely cited by the Examiner for having the USB

dual host controller chip 139 which has the bus interface unit 140, USB arbiter 145, and a pair of USB host controllers 150, 155 made on a single chip. The USB dual host controller chip 139 of Abramson, et al. is not however a memory card and fails to include SD interface, USB interface, and a controller for judging which one of the interfaces to actuate.

While the present invention is a memory card integrating functions of the USB interface which has the configuration shown in Fig. 2 wherein the memory chip has a CD interface 20, USB interface 22, and a controller 24 for selecting one of the SD and USB interfaces to be connected to the USB connector.

Further, in the present invention, this is a controller 24 embedded in the memory chip 14 which selects which of the interfaces, SD interface or USB interface, to actuate.

In contrast to the present invention, and similar to Takahachi Patent, in the Abramson, et al. reference, it is a decision of the external arbiter, such as the PCI arbiter in the host bridge 115, which is not a part of the controller chip 139, to independently determine which of the USB host controllers 150 or 155 the USB arbiter 145 is to actuate.

The Examiner suggested the combination of Takahachi with Abramson, et al. to result in the combination of elements defining the present invention. It is respectfully submitted that absent the Applicant's disclosure, there is no motivation for combining the USB dual host controller chip 139 of Abramson, et al. (which does not pertain to a

memory card having added functions of the USB interface, and where the arbiter on the chip 139 fails to judge which one of the USB controllers to actuate) with Takahachi (which itself fails to provide a selection of actuation of a memory controller or USB interface by controlling means embedded into the memory chip). It can only be thought an improper use of "hindsight", using Applicant's disclosure as a "blueprint" for the combination, that the Examiner suggests such a combination of references, Abramson, et al., and Takahachi.

Arguendo, even if teachings of Abramson, et al. and Takahachi are combined, it is believed that the combination of elements of the invention of the subject Application, as now claimed, still provides patentable distinction over the structure resulting from the Examiner's suggested combination. None of the references cited by the Examiner taken singly or in combination thereof, disclose, suggest, or render obvious --a memory card integrating functions of the USB interface in which a controller embedded into the memory chip selects a respective one of said SD (or MS or memory card) control interface and USB control interface for actuation, thereby controlling the coupling of the memory card to a USB connector--. This feature simply is not taught by the references cited by the Examiner. Claims 1, 7, and 13 now clearly present (inter alia) this feature. As Claims 1, 7, and 13 clearly direct themselves to the concept and structure where the controller embedded in the memory chip selects a respective one of the SD (or MS, or memory card) control interface and USB control interface for actuation, these Claims 1,

7, and 13 are believed to be patentably distinct over the cited prior art, taken singly or in combination. Accordingly, Claims 1, 7, and 13 as amended are believed to be allowable; and the same is respectfully urged.

Claims 2-5 dependent on Claim 1, Claims 8-11 dependent on Claim 7, and Claims 14-16 dependent on Claim 13 have been amended to correct the language thereof. These Claims are believed each to add further limitations that are patentably distinct in addition to being dependent upon what is now believed to be a patentable base Claim, and therefore, allowable for at least the same reasons.

For all of the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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